A 40-Gbit/s Optical Repeater Circuits using InAlAs/InGaAs HEMT Digital IC Chip Set

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abstract

This paper describes an InAlAs/InGaAs HEMT digital IC chip set which includes a multiplexer, demultiplexer, decision circuit, and frequency divider. Electrically multiplexed and demultiplexed 40-Gbit/s transmission is successfully performed.

1. Introduction

High speed electrical circuits are key components in the next generation of time division multiplexing (TDM) optical fiber communication systems [1]. This paper proposes an InP-based digital IC Chip Set incorporating a 2:1 multiplexer (MUX), 1:2 demultiplexer (DEMUX), decision circuit (DEC), and 1/2 frequency divider (DIV) as a candidate for these systems. The authors successfully demonstrate 40-Gbit/s electrical TDM transmission and further advances in circuit design that enable operation beyond 40 Gbit/s.

2. InP HEMT for Digital ICs

Many electrical ICs reported for over 10-Gbit/s transmission systems are fabricated as Si-bipolar, GaAs MESFET, HBT, and HEMT. Figure 1 shows the empirical relationship between the maximum operating speed of D-F/Fs (or DEC) and the device figure of merit [2]. Faster devices are the key to achieving a higher bit rate. InP HEMT offers the highest f_T and f_{max} of all semiconductor devices and is a good candidate to achieve digital ICs that operate at over 40 Gbit/s. In fact, our first trial ICs, 2:1 MUX and 1:2 DEMUX, operate at over 40-Gbit/s [3] , and have successfully achieved 40 Gbit/s, 300 km transmission [1,4] even though they represent a preliminary stage of HEMT design. Novel circuit design technology is another key. As shown in Fig. 1, the HLO [5] and super-dynamic type D-F/F [6] can achieve bit rates 1.5 times and 2 times as fast as a conventional master-slave D-F/F, respectively. The combination of the InP HEMT process and the circuit design technology promises ultrafast digital ICs for 40-Gbit/s and beyond optical repeater circuits.

3. Device Technology

The device we employed for ICs is a 0.1-μm gate InAlAs/InGaAs HEMT [7,8]. A novel recess-etch stopper reduces the standard deviation to around 30 mV of the threshold voltage (V_{th}) in a 2-inch wafer and enables the use of HEMTs in digital ICs. Schottky diodes using the additional InAlAs/n-InAlAs layers on the HEMT layers were used as level shift diodes because of their small size and low resistance. The measured f_T and transconductance, g_m, are 174 GHz and 950 mS/mm, respectively. The f_{max} was estimated to be 400 to 500 GHz from the equivalent circuit parameters.

4. Circuit Design

As the operating speed of a D-F/F increases, faster data and clock buffers are indispensable. Figure 2 shows the circuit configurations of the buffers we used. The data buffer employs capacitive feedback at the differential buffer [9] and capacitive peaking at the source follower. The capacitive feedback cancels the influence of the parasitic capacitance of C_{gd}, and the capacitive peaking compensates the loss of the source follower in the high frequency region. The data amplifiers we used also employ the same configuration except for the source follower at the input stage. The clock buffer consists of a two-stage inductor peaking differential buffer. A capacitively coupled resistive divider was introduced as a low-loss, passive RF level shifter instead of source followers.

The core of the DEC is the super-dynamic D-F/F shown in Fig. 3. The super-dynamic D-F/F is characterized by a source-coupled negative feedback pair (SCNFP) inserted in the first-level latching differential pair in a cascode manner. The SCNFP drastically reduces the effective logic swing and increases F/F operating speed. The circuit block diagram of the DEC and other ICs, 2:1 MUX, 1:2 DEMUX, DIV are shown in Fig. 4.

The fabricated IC chip set was embedded in a

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package that can accommodate up to six RF ports with V-band connectors [10] . The package minimizes the inner cavity in order to shift the cavity resonance outside the transmission bandwidth. The ICs are mounted on a thin-film multilayer interconnection substrate using ribbon wire.

5. IC Performances

On wafer and packaged IC performances were measured. As the signal source, a complementary PRBS from a pulse pattern generator (PPG), one of which was delayed, was multiplexed by a GaAs MESFET MUX and the HEMT MUX module. Figure 5 shows the eye patterns observed by a sampling oscilloscope. The maximum operating speeds and power dissipation are shown in Table 1.

6. 40-Gbit/s, 300-km transmission

We fabricated an optical repeater circuit using the IC modules and performed 40-Gbit/s transmission. The experimental setup is shown in Fig. 6. Four-channel 10-Gbit/s PRBS (2^7-1) signals, delayed by a quarter data period against each other , were generated from a PPG. They were multiplexed to 20 Gbit/s using two GaAs MESFET MUXs, and further multiplexed up to 40 Gbit/s using the MUX module. The 40-GHz optical pulse train from a monolithic mode-locked laser diode (ML-LD) module [11] was encoded by a $LiNbO_3$ Match Zehnder modulator [12] . The modulated 40-Gbit/s RZ optical signal was amplified by an EDFA and injected into the transmission line. The transmission line was comprised of four 75-km long dispersion shifted fibers (DSFs) connected by three EDFAs. Each EDFA accommodates a dispersion compensator to cancel the dispersion of the transmission section. The transmitted signal was amplified by another EDFA, followed by a dispersion equalizer module [13] . The signal was received by the optical receiver module we newly developed that comprises a waveguide type pin-PD and a GaAs MESFET distributed amplifier [14]. The received signal was fed into the DEC module, then demultiplexed to 10 Gbit/s by another DEC module and a Si-bipolar DEC to measure bit error rate (BER). The observed 40-Gbit/s eye patterns are shown in Fig. 7. There is the inter symbol interference (IMI) of the received eye pattern (Fig. 7 (c)). The BER performance of the four 10-Gbit/s channels in the 40-Gbit/s data stream was measured by adjusting the clock timing of D-F/Fs and is shown in Fig. 8. The average receiver sensitivities at the BER of 10^{-9} before and after transmission were -24.8 dBm (δ=0.2 dB) and -24.3 dBm (δ=0.6 dB), respectively. A small power penalty of 0.5 dB after 300-km transmission was obtained. The sensitivity can be improved by reducing the ISI of the receiver module.

Conclusion

We have developed optical repeater circuits using InAlAs/InGaAs HEMTs digital IC modules and performed 40-Gbit/s, 300-km transmission. By taking advantage of the newly designed digital IC Chip Set, we anticipate repeater circuit performance beyond 40-Gbit/s.

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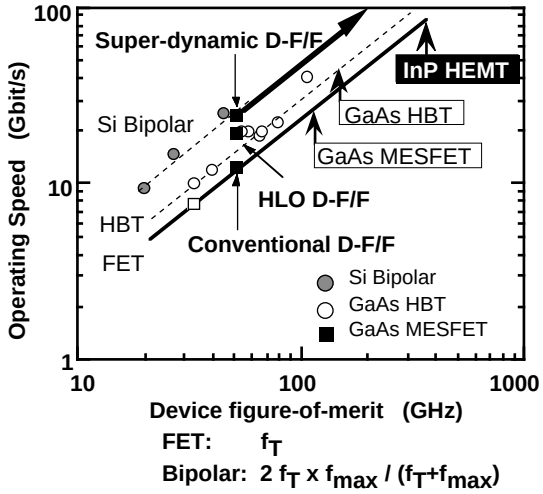


Fig. 1. Relationship between operating speed of D-F/Fs and device figure-of-merit.

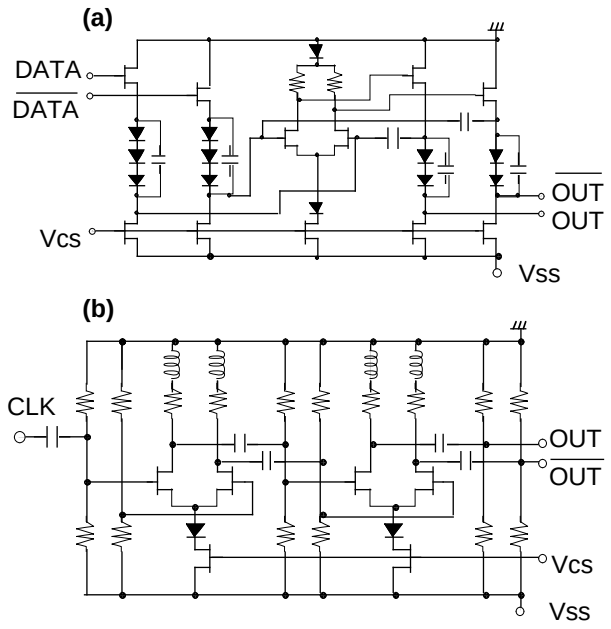


Fig. 2. Circuit configuration of data buffer (a), and clock buffer (b).

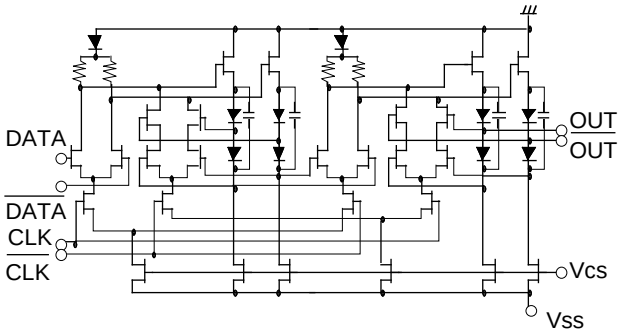
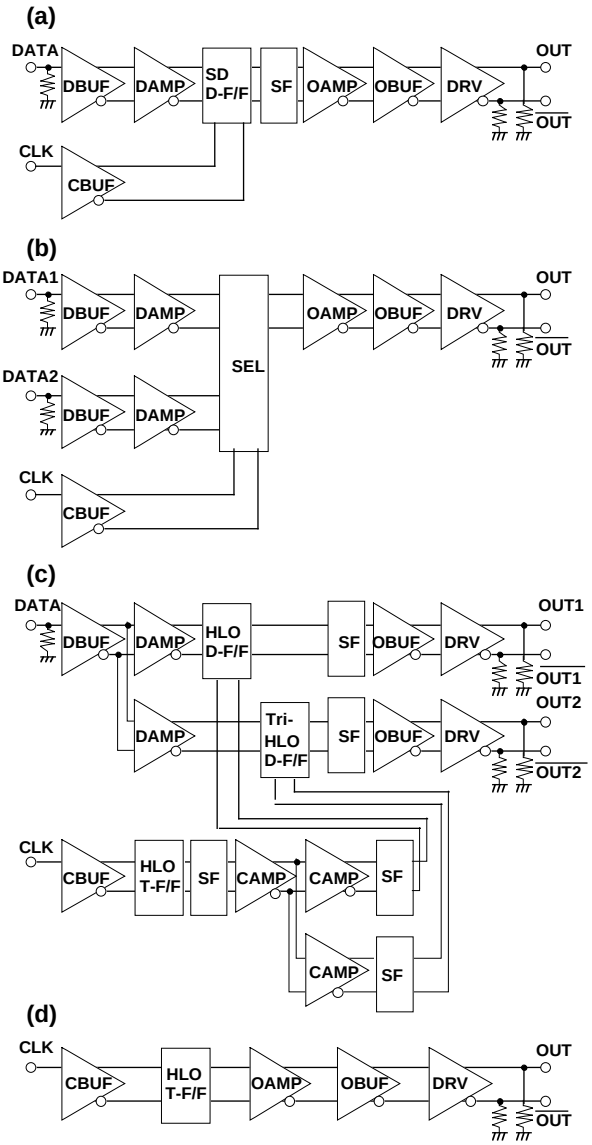


Fig. 3. Circuit configuration of super-dynamic D-F/F.



DBUF: data input buffer, DAMP: data input amplifier,
OBUF: data output buffer, OAMP: data output amplifier,
CBUF: clock input buffer, CAMP: clock amplifier,
DRV: driver, SF: source follower, SD: super-dynamic,
SEL: selector, Tri: 3-stage

Fig. 4. Circuit configuration of (a) DEC, (b) 1:2 MUX, (c) 1:2 DEMUX, (d) DIV.

Table 1. Operating speed and power dissipation of IC chip set

IC	module	on wafer	power dissipation
DEC	15 - >40 Gbit/s	15- 46 Gbit/s	1.7 W
2:1 MUX	1 - ~ 64 Gbit/s	1 - 52 Gbit/s	2.2 W
1:2 DEMUX	2 - 40 Gbit/s	2 - 40 Gbit/s	3.8 W
DIV	2 - 46 GHz	2 - 45 GHz	1.1 W

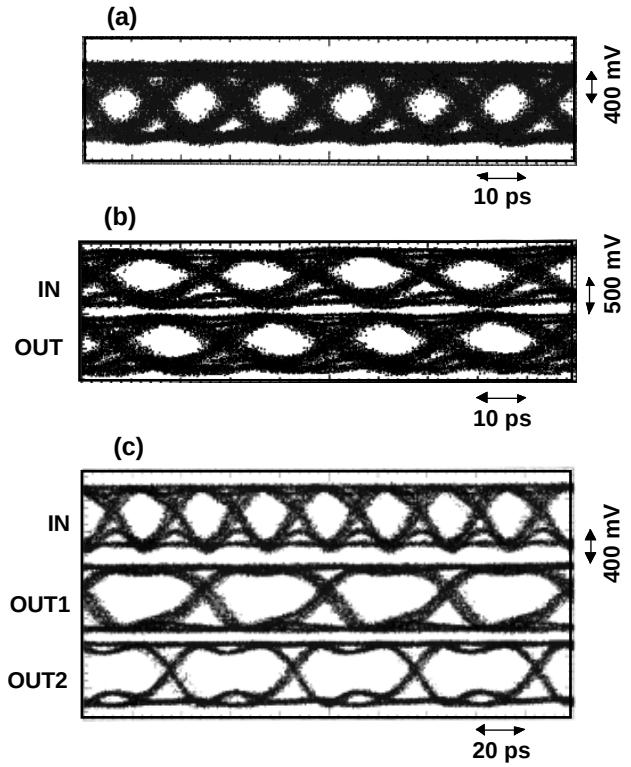
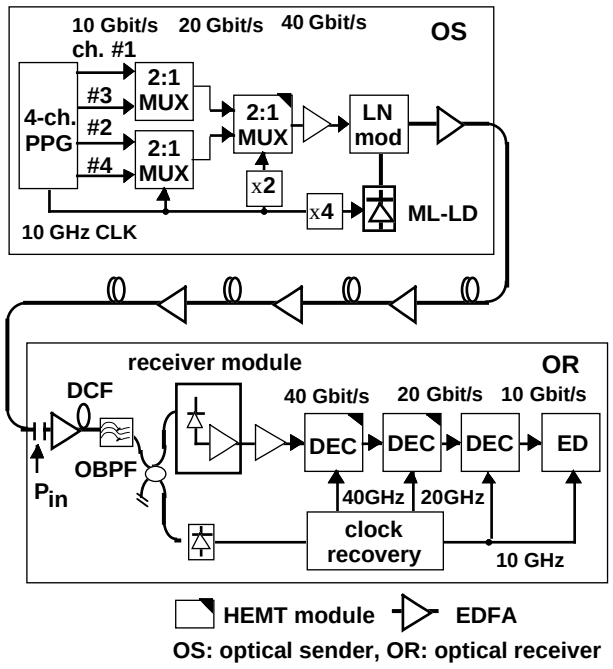


Fig. 5. Output eye patterns
(a) 2:1 MUX (on wafer), 64 Gbit/s, (2^{31}-1) PRBS
(b) DEC module, 46 Gbit/s, (2^{15}-1) PRBS



(c) 1:2 DEMUX module, 40 Gbit/s (2^{23}-1) PRBS input

Fig. 6. Experimantal setup of 40-Gbit/s, 300-km transmission.

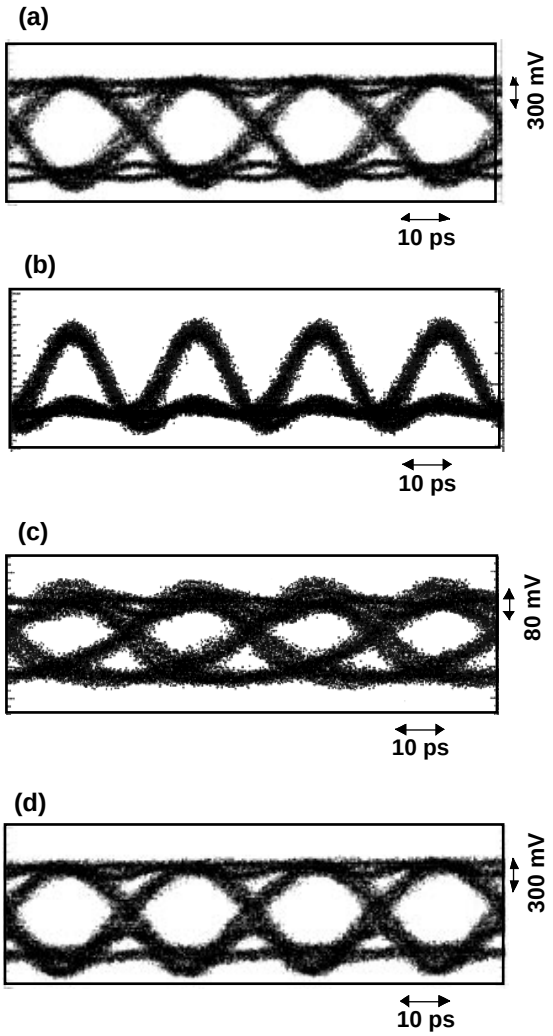


Fig. 7. 40-Gbit/s eye patterns of (a) 2:1 MUX, (b) OS, (c) receiver module, and (d) DEC.

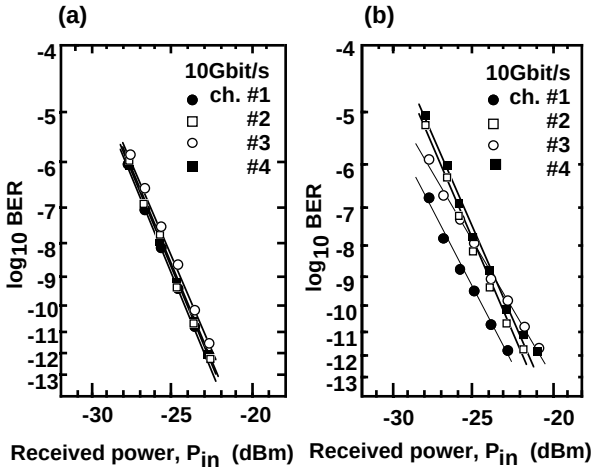


Fig. 8. Bit error rate performance at 40 Gbit/s; back-to-back (a), and after 300 km transmission (b).